AMENDMENTS TO CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1-3. (Canceled)

4. (Currently Amended) A semiconductor memory device comprising:

a plurality of bit lines that are adjacent to each other;

~~a plurality of gates intersecting with said bit lines;~~

a plurality of active areas, ~~each of which is connected to one of said bit lines~~, of which a first active area is connected with a bit line and second active area is connected with another bit line, said two bit lines being adjacent to each other, and each active area having two cells;

a plurality of work lines, each word line being connected with one corresponding cell;

a plurality of deep trenches, ~~at least~~ one of which communicates with ~~only two different active areas which are respectively connected with two adjacent two of said bit lines~~ one of the two cells located in the first active area and one of the two cells located in the second active area, so as to measure a leakage current between ~~said two different~~ the first and second active areas.

5. (Previously Presented) The device as claimed in Claim 4, wherein ~~the cross section of said deep trench communicates with said two different active areas~~ two different word lines respectively control two different cells in one active area.

6. (Canceled)